

WHAT IS CLAIMED IS:

1. A method of converting an analog signal into a digital signal, comprising:
receiving the analog signal;
sampling the analog signal at a plurality of points in time to produce a sampled
5 signal which represents the analog signal;
incorporating into said sampling step a filtering operation which filters the analog
signal such that the sampled signal represents a filtered version of the analog signal; and
producing the digital signal from the sampled signal.

10 2. The method of Claim 1, wherein said filtering operation is a finite impulse
response (FIR) filtering operation.

3. The method of Claim 2, wherein said finite impulse response filtering
operation is a linear phase finite impulse response filtering operation.

15 4. The method of Claim 1, wherein said incorporating step includes using a
switched capacitor filter bank to implement the filtering operation.

5. The method of Claim 4, wherein said using step includes controlling
switches in the switched capacitor filter bank in a first manner to realize a first filtering
20 operation.

6. The method of Claim 5, wherein said using step includes controlling switches in the switched capacitor filter bank in a second manner to realize a second filtering operation.

5 7. The method of Claim 1, wherein said sampling step includes charging more than one capacitor simultaneously.

8. The method of Claim 7, wherein said sampling step includes dumping charges from more than one capacitor simultaneously.

10 9. The method of Claim 1, wherein said sampling step includes dumping charges from more than one capacitor simultaneously.

10. The method of Claim 1, wherein said sampling step includes dumping
15 from a first capacitor to a charge summing node a first charge that represents a first sample of the analog signal while also simultaneously dumping from a second capacitor to the charge summing node a second charge that represents a second sample of the analog signal which timewise preceded the first sample in the analog signal.

11. The method of Claim 1, wherein the analog signal is a communication signal carried on a frequency channel, and wherein the filtering operation filters interfering frequencies out of the analog signal.

5 12. An apparatus for use in converting an analog signal into a digital signal, comprising:

an input for receiving the analog signal;

a sampler coupled to said input for performing on the analog signal a sampling operation wherein the analog signal is sampled at a plurality of points in time to produce

10 a sampled signal which represents the analog signal;

a filter coupled to said sampler for incorporating into said sampling operation a filtering operation which filters the analog signal such that the sampled signal represents a filtered version of the analog signal; and

15 an output coupled to said sampler for providing the sampled signal to a circuit which can produce therefrom the digital signal.

13. The apparatus of Claim 12, wherein said filtering operation is a finite impulse response (FIR) filtering operation.

20 14. The apparatus of Claim 12, wherein said finite impulse response filtering operation is a linear phase finite impulse response filtering operation.

15. The apparatus of Claim 12, wherein said filter includes a switched capacitor filter bank.

16. The apparatus of Claim 15, including a switch controller coupled to said
5 switched capacitor filter bank for controlling switches in said switched capacitor filter bank to realize a desired filtering operation.

17. The apparatus of Claim 12, wherein said sampler includes a first switched capacitor network having a first capacitor for selectively storing and dumping charge.

10 18. The apparatus of Claim 17, wherein said filter includes a second switched capacitor network having a second capacitor for selectively storing and dumping charge.

15 19. The apparatus of Claim 18, wherein said first and second capacitors are connected to a common node.

20 20. The apparatus of Claim 18, wherein said first switched capacitor network includes a switch connected to said first capacitor for use in charging said first capacitor, and wherein said switch is also connected to said second capacitor for use in charging said second capacitor.

21. The apparatus of Claim 18, wherein said second switched capacitor network includes a plurality of capacitors for selectively storing and dumping charges.

22. The apparatus of Claim 18, including a switch controller coupled to said
5 first and second switched capacitor networks for controlling switches in said first and second switched capacitor networks such that said first and second capacitors store respective charges simultaneously.

23. The apparatus of Claim 22, wherein said switch controller is further for
10 controlling switches in said first and second switched capacitor networks such that said first and second capacitors dump respective charges simultaneously.

24. The apparatus of Claim 23, wherein said charge dumped from said first capacitor represents a first sample of the analog signal, and wherein said charge dumped
15 from said second capacitor represents a second sample of the analog signal which timewise preceded the first sample in the analog signal.

25. The apparatus of Claim 24, wherein said first and second capacitors are connected to a common node, and including a switch coupled to said switch controller
20 for, under control of said switch controller, selectively connecting said common node to an input of a further stage of said apparatus.

26. The apparatus of Claim 12, wherein the analog signal is a communications signal carried on a frequency channel, and wherein said filtering operation filters interfering frequencies out of the analog signal.

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27. The apparatus of Claim 12, including said circuit coupled to said output, and wherein said circuit includes a portion of said filter.

28. The apparatus of Claim 27, wherein said portion of said filter includes an integrator circuit.

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29. A communication receiving apparatus, comprising:
an input for receiving a communication signal at a first frequency;
a mixer coupled to said input for mixing said communication signal down from
said first frequency to a second frequency; and
an analog-to-digital conversion apparatus coupled to said mixer for converting
said second frequency signal from analog format to digital format, said analog-to-digital
conversion apparatus including a sampler coupled to said mixer for performing on said
second frequency signal a sampling operation wherein said second frequency signal is
sampled at a plurality of points in time to produce a sampled signal which represents said
second frequency signal, a filter coupled to said sampler for incorporating into said

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sampling operation a filtering operation which filters said second frequency signal such that the sampled signal represents a filtered version of said second frequency signal, and circuitry coupled to said sampler for receiving said sampled signal and producing therefrom a digital signal.

5 30. The apparatus of Claim 29, wherein said circuitry includes an integrator circuit.

 31. The apparatus of Claim 30, wherein said integrator circuit is a single-ended integrator circuit.

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 32. The apparatus of Claim 29, wherein said circuitry includes delta sigma modulation circuitry.